

FIG. 1.
(PRIOR ART)

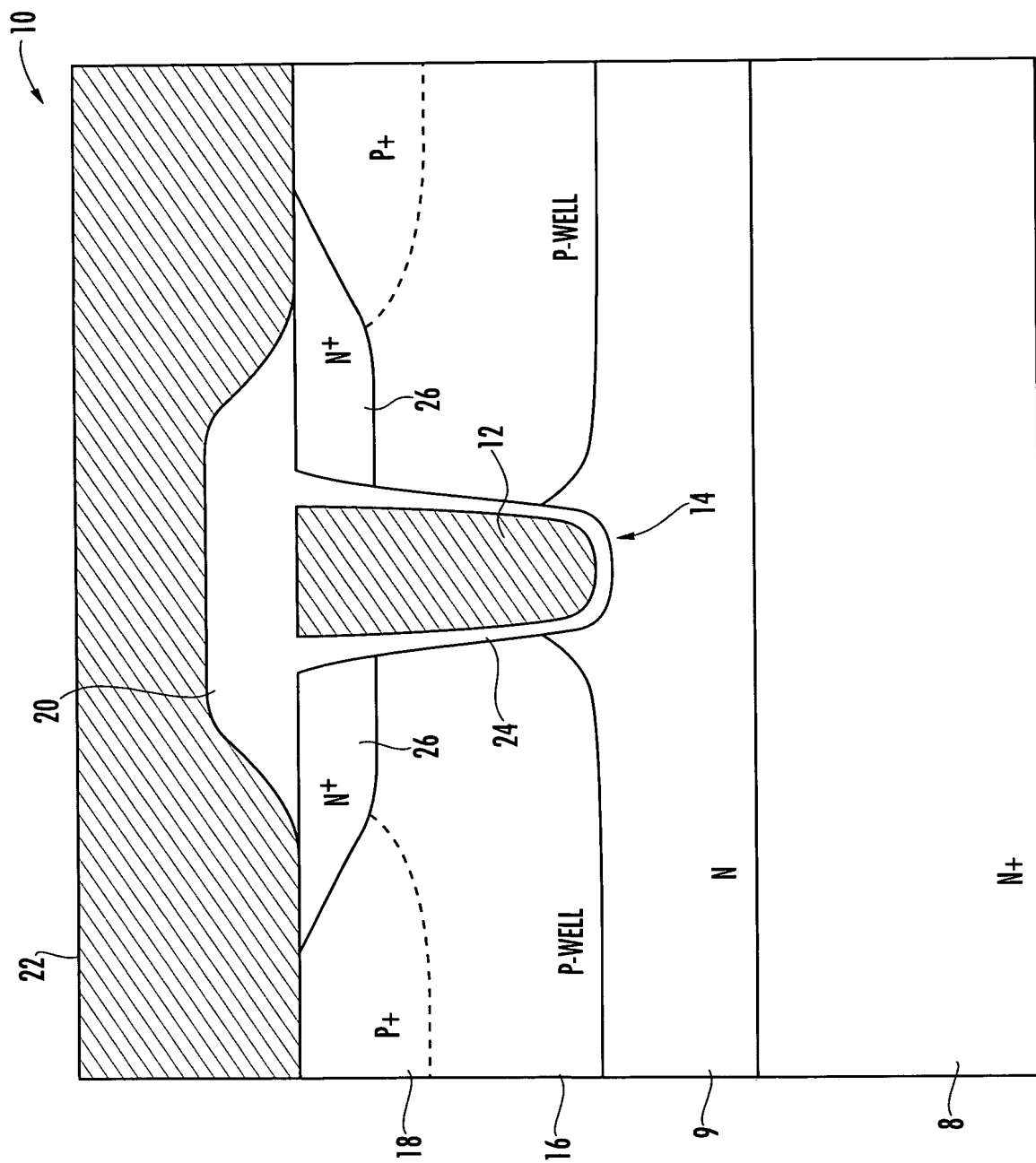
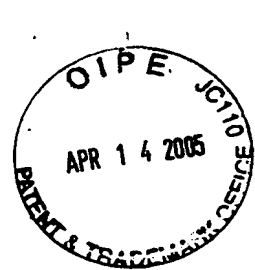


FIG. 2.
(PRIOR ART)



3/11
REPLACEMENT SHEET

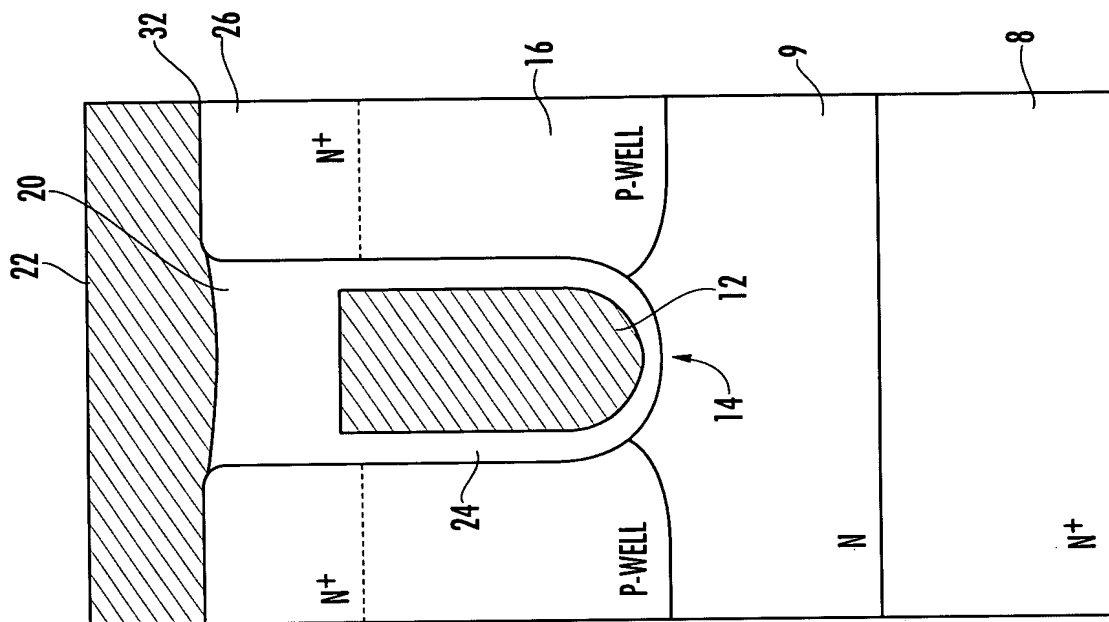


FIG. 3b.
(PRIOR ART)

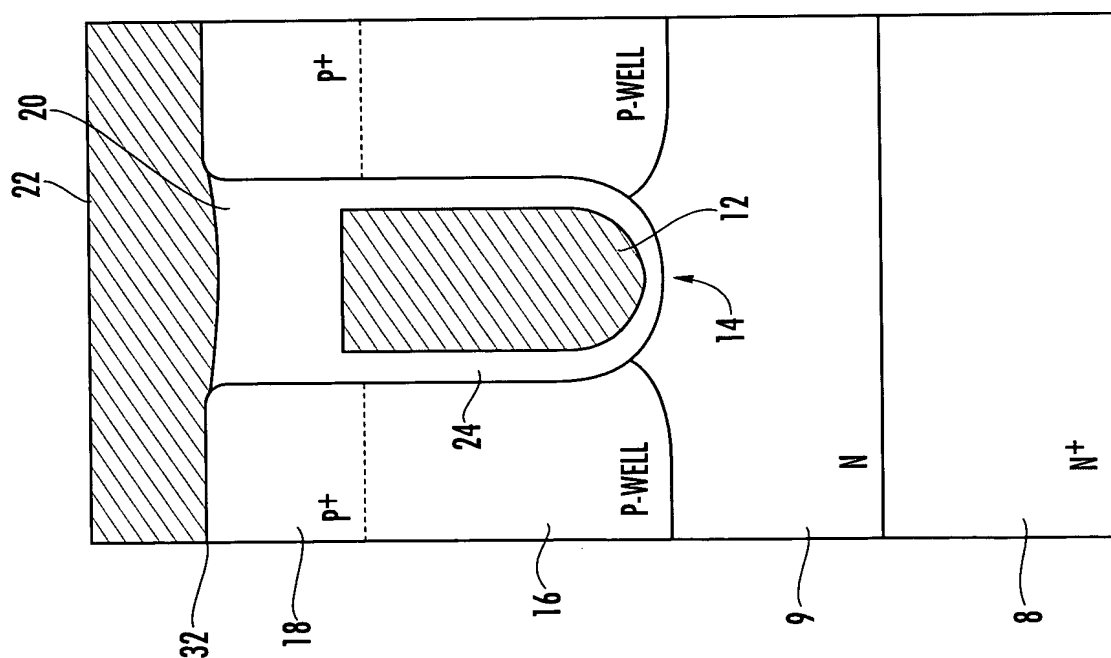


FIG. 3a.
(PRIOR ART)



4/11
REPLACEMENT SHEET

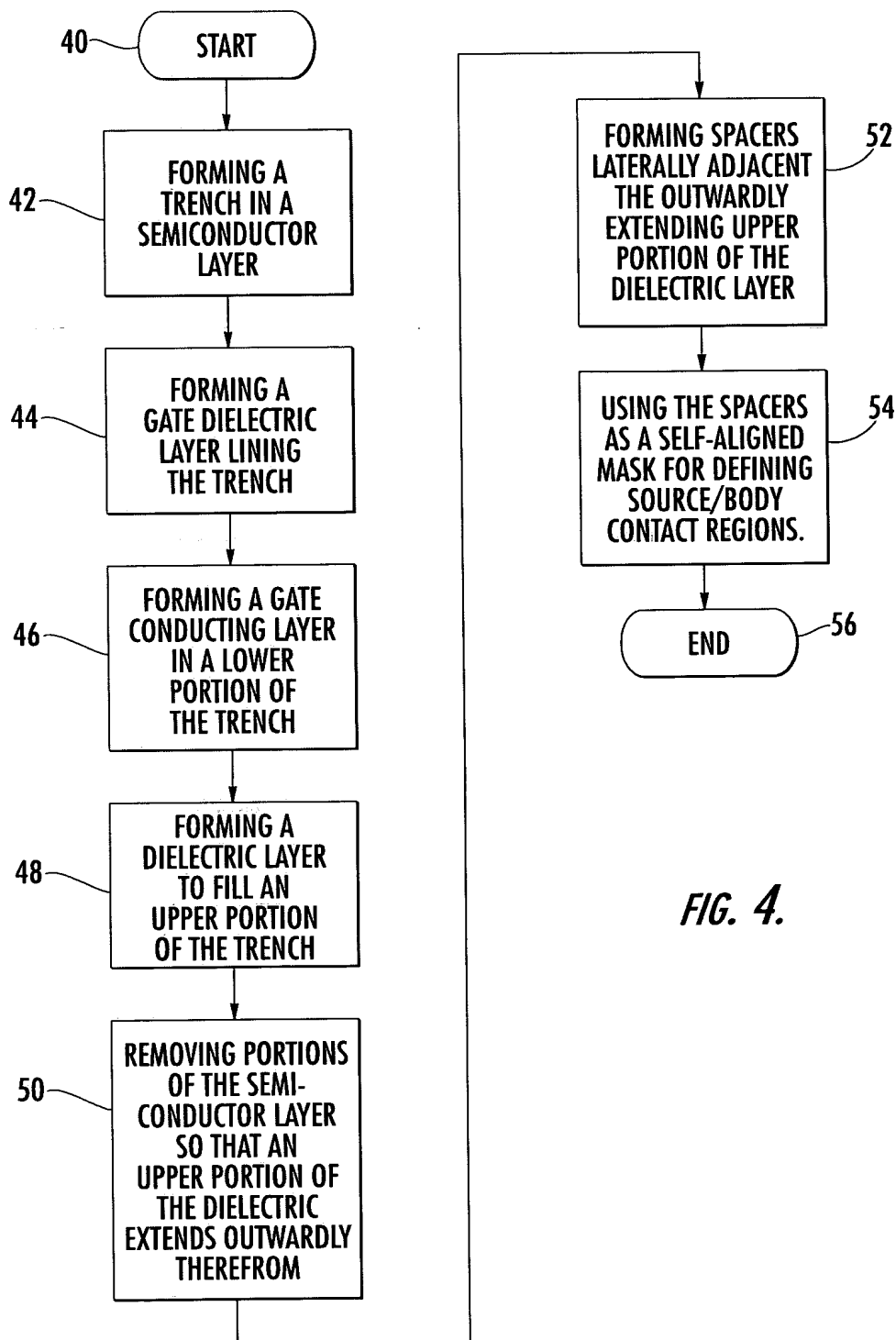
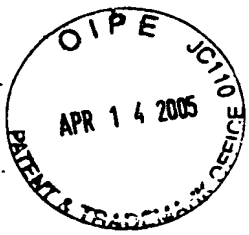


FIG. 4.



5/11
REPLACEMENT SHEET

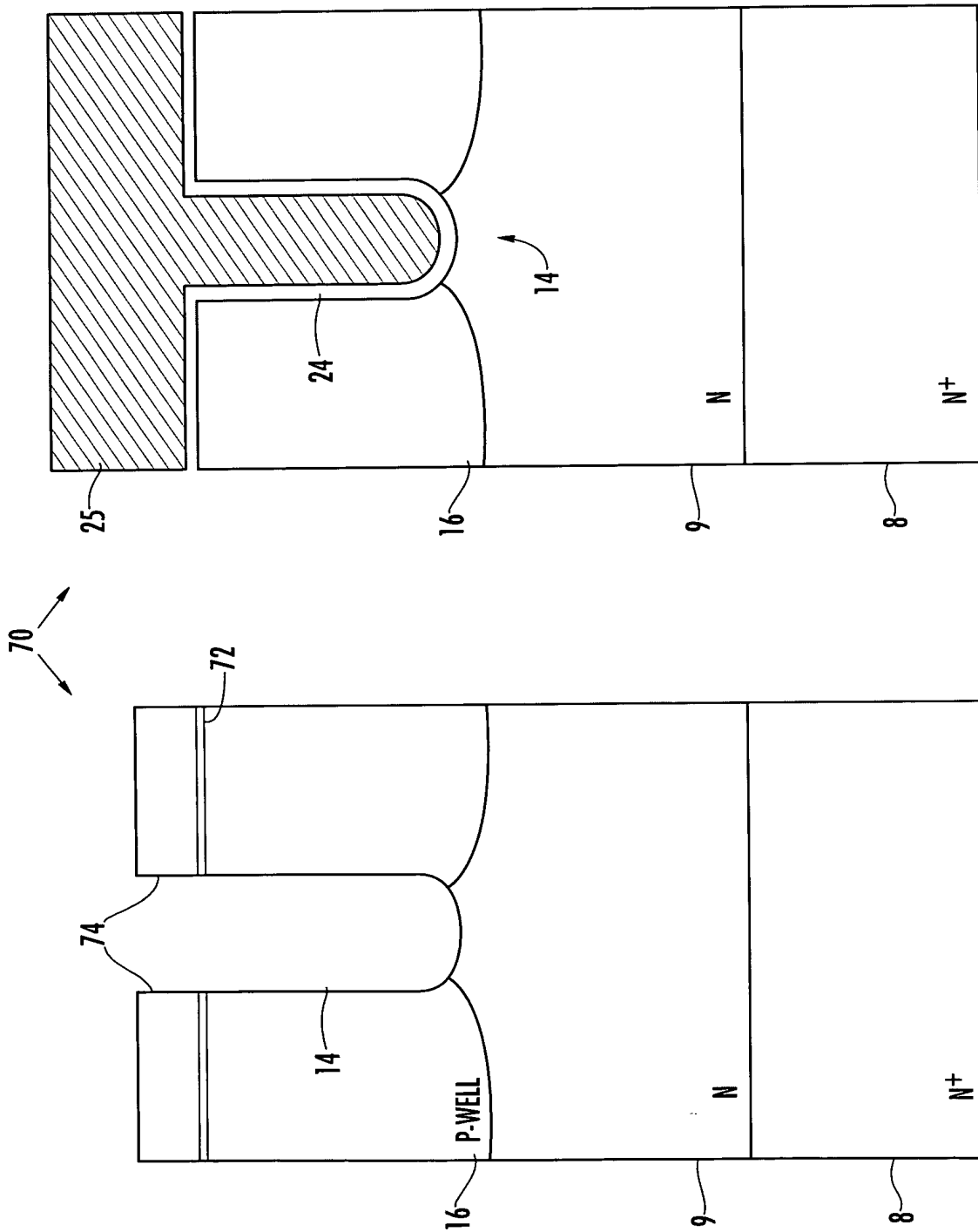
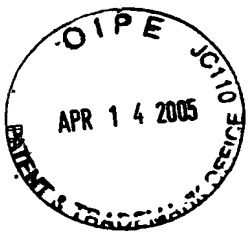


FIG. 6.

FIG. 5.



6/11
REPLACEMENT SHEET

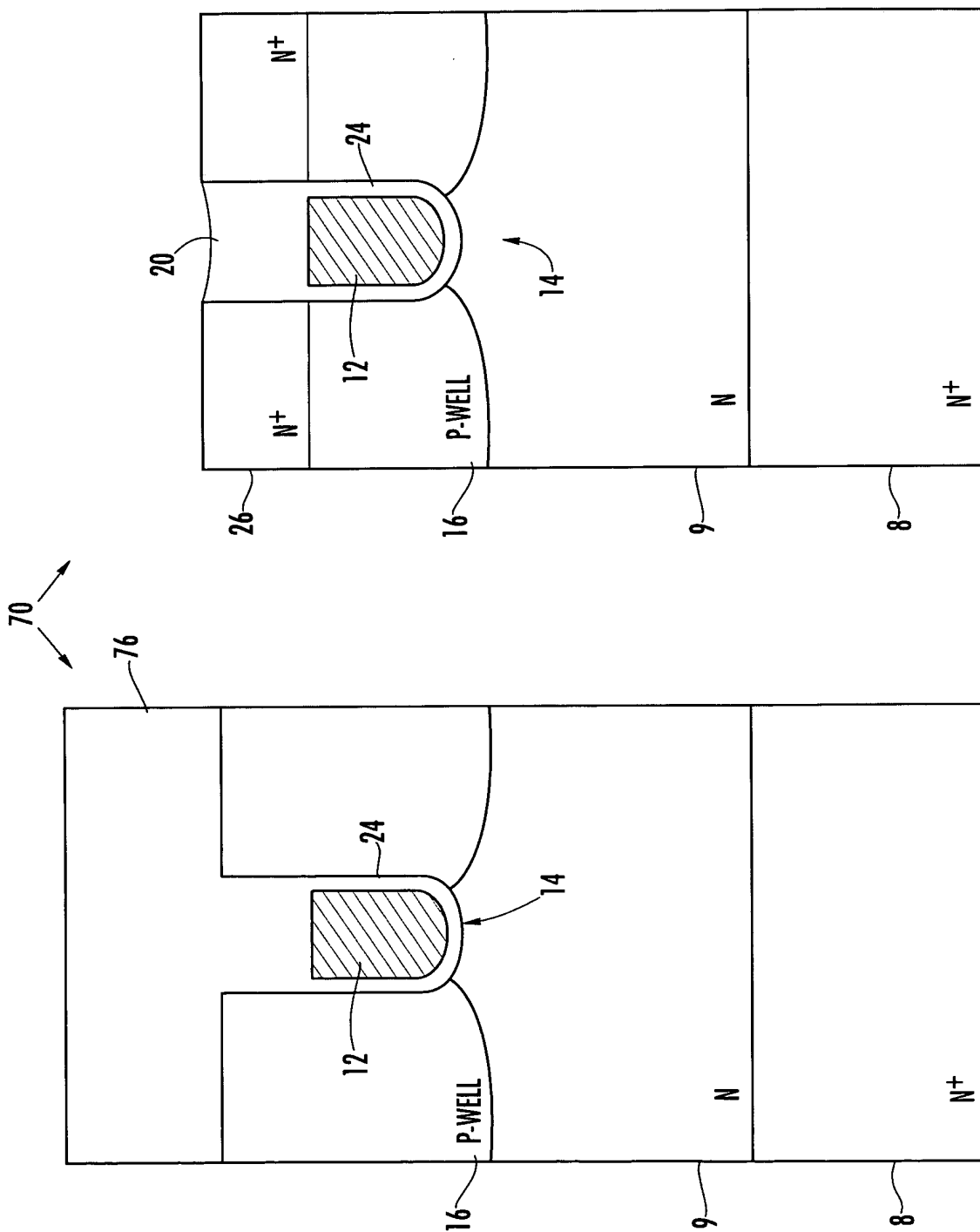
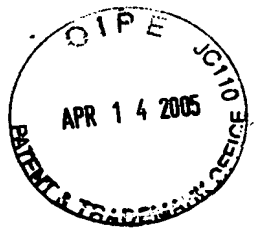


FIG. 8.

FIG. 7.

This diagram shows a cross-sectional view of a semiconductor device. A central gate structure, labeled 20, is positioned on top of a substrate. The gate structure includes a gate dielectric layer 12 and a gate electrode 16. The substrate is divided into several regions: an N⁺ region 26 on the left, a P⁺ region 82 in the center, and an N⁺ region 80 on the right. A P-WELL region 16 is located beneath the gate structure. The substrate is also labeled with 8 and 9. The gate structure is labeled with 80 and 82.



8/11
REPLACEMENT SHEET

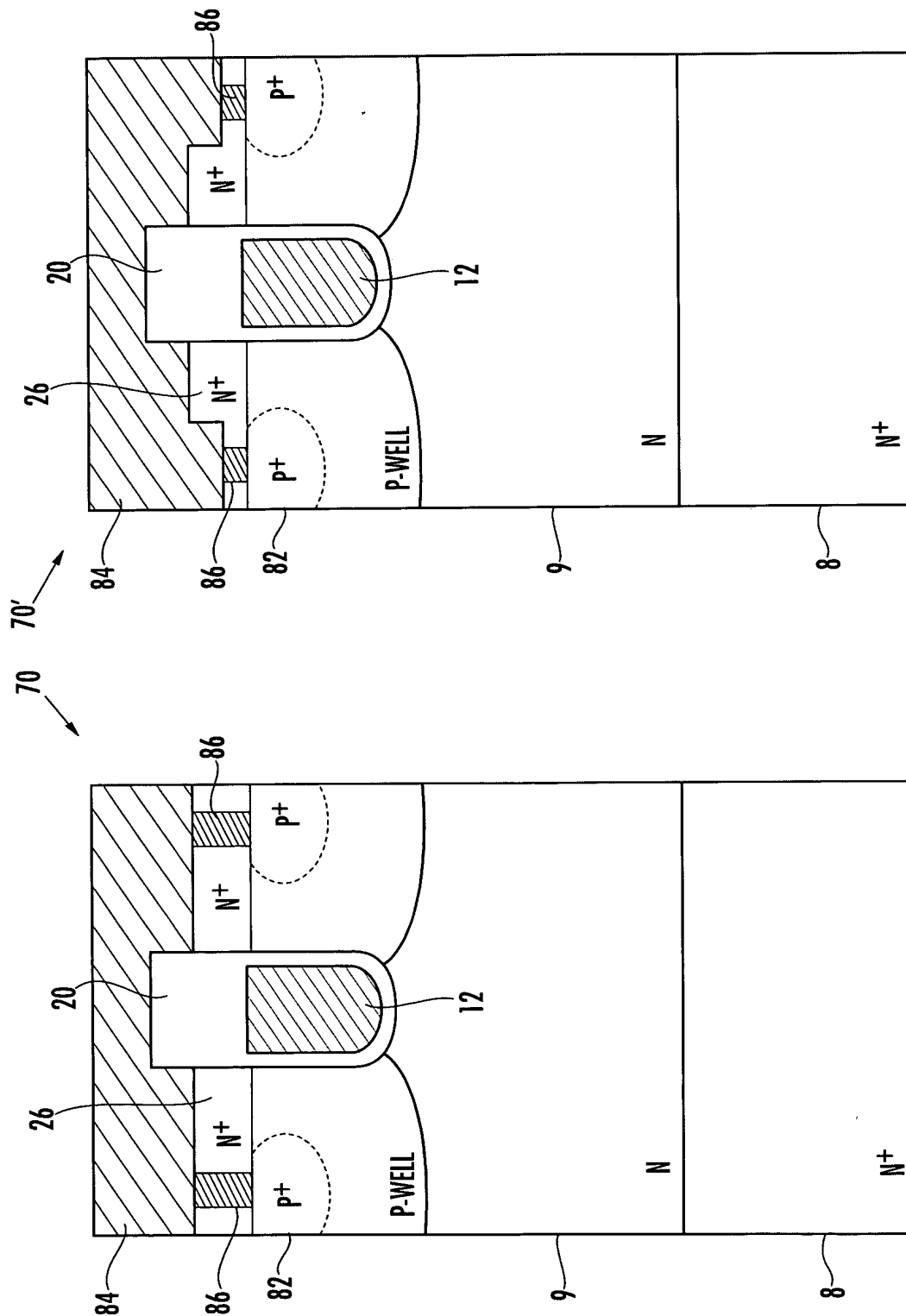


FIG. 12.

FIG. 11.



9/11
REPLACEMENT SHEET

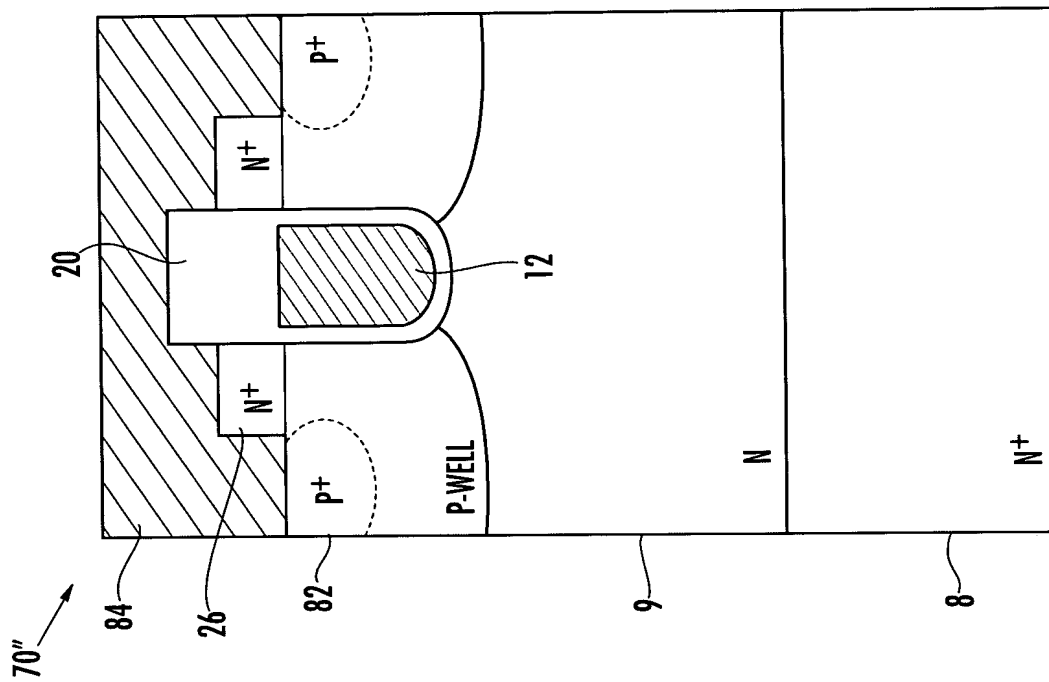


FIG. 13.



10/11
REPLACEMENT SHEET

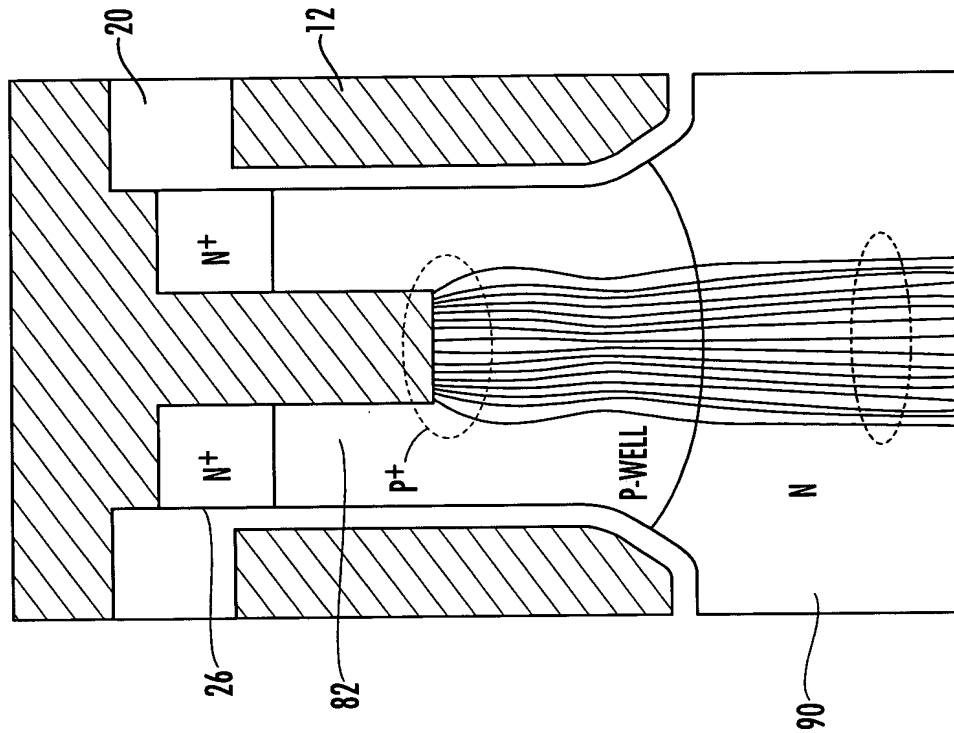


FIG. 15.

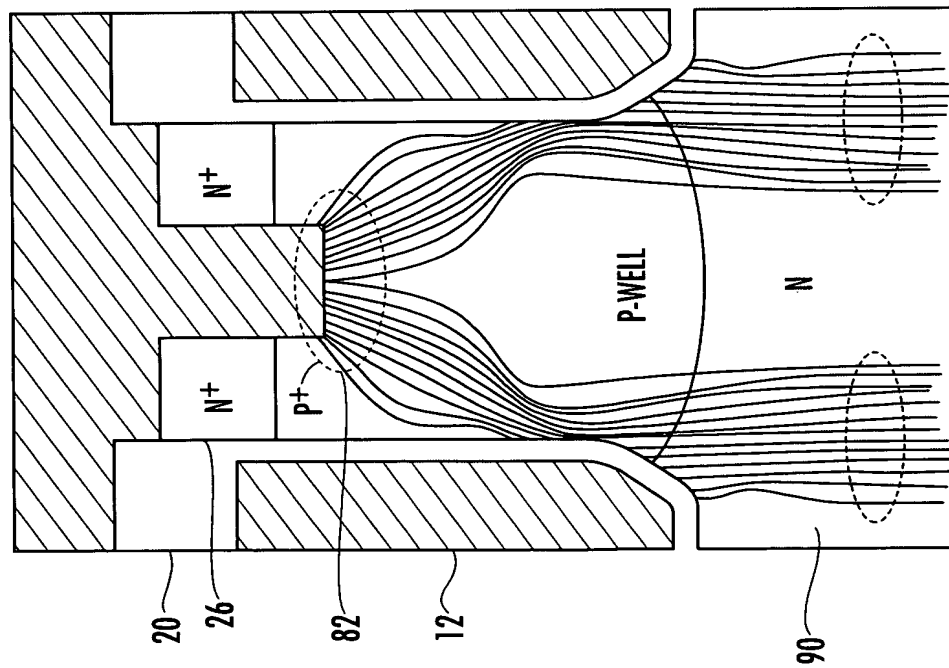
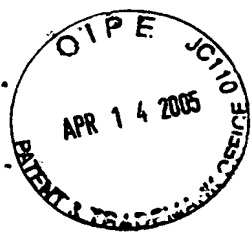


FIG. 14.



11/11
REPLACEMENT SHEET

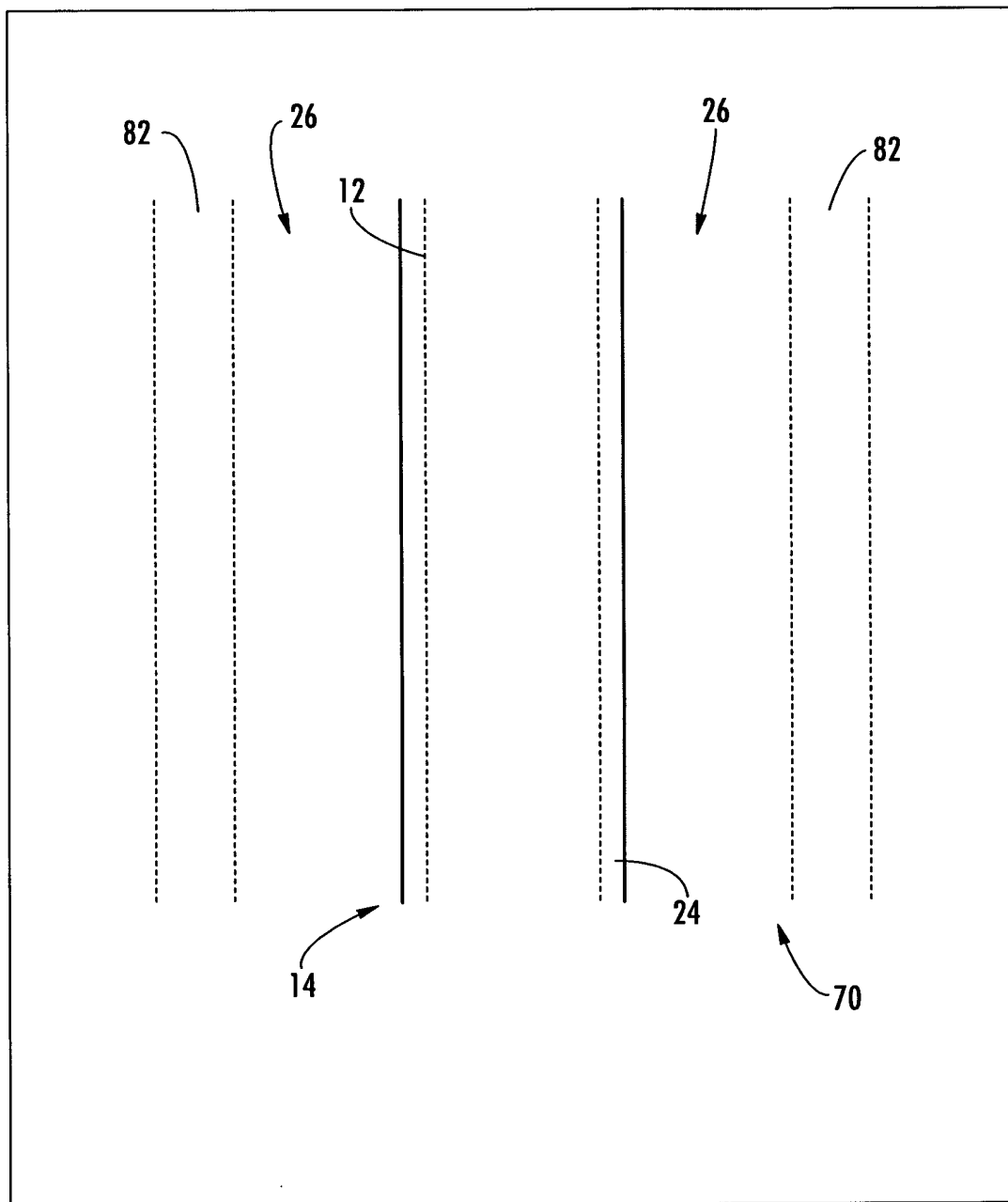


FIG. 16.